CLAIMS

We Claim:

1. A method of improving yield in a multiple way associative cache memory having a plurality of cache blocks each corresponding to one of the multiple ways, the method comprising:

determining whether a defect exists in any of the cache blocks; and

for each way, selectively disabling the way if the corresponding cache block is defective.

2. The method of Claim 1, further comprising:

for each way, storing a way select value indicative of whether the corresponding cache block is defective.

3. The method of Claim 1, further comprising:

operating the remaining, non-disabled cache blocks as a less-associative cache memory.

4. The method of Claim 1, wherein during a cache read operation the disabling step comprises:

forcing a comparison between a requested tag address and tags corresponding to cache lines in the disabled cache block to a mismatch condition so that the disabled cache block is not selected for the cache read operation.

5. The method of Claim 4, wherein the forcing step comprises:

comparing the requested tag address with tags corresponding to the disabled cache block;

generating, for each cache block, a match signal indicating the results of the comparing step; and

gating the match signals with corresponding way select values to selectively force the mismatch condition for comparison results corresponding to the disabled cache block.

6. The method of Claim 4, wherein during a cache write operation the disabling step comprises:

configuring a cache replacement algorithm to never select the disabled cache block.

7. A method of improving yield in an N way associative cache memory having N cache blocks corresponding to the N ways, the method comprising:

determining whether a defect exists in a cache block;

disabling the cache block if there is a defect in the cache block; and

operating the remaining cache blocks as an N-1 way associative cache memory.

8. The method of Claim 7, further comprising:

storing a plurality of way select values, each indicating whether a corresponding cache block is to be disabled.

9. The method of Claim 8, wherein during a cache read operation the disabling step comprises:

forcing a tag comparison corresponding to the disabled cache block to a mismatch condition.

10. The method of Claim 9, wherein the forcing step further comprises:

comparing a requested tag address with tags

corresponding to the disabled cache block;

generating a match signal in response to the comparing step; and

gating the match signal with a corresponding way select value to selectively force the mismatch condition.

11. A multiple-way associative cache memory, comprising:

a plurality of cache blocks, each having a number of cache lines to store data;

a plurality of tag arrays, each storing a number of tags for associated data in a corresponding one of the plurality of cache blocks; and

select means connected to both the cache blocks and the tag arrays, the select means configured to selectively disable one or more of the plurality of cache blocks.

12. The cache memory of Claim 11, wherein the select means comprises:

a plurality of memory devices, each for storing a way select value for a corresponding cache block;

a plurality of gating circuits, each having a first input terminal coupled to receive a match signal from a corresponding tag array, a second input terminal coupled to receive a corresponding way select value, and having an output terminal to provide a gated match signal for a corresponding cache block.

13. The cache memory of Claim 12, further comprising:

an encoder circuit having a plurality of input terminals coupled to receive the gated match signals for corresponding cache blocks, and having an output terminal to provide a select signal; and

a multiplexer having a plurality of input terminals coupled to receive data from corresponding cache blocks, an output terminal to provide output data, and a control terminal to receive the select signal.

14. The cache memory of Claim 13, wherein the select signal selects which cache block provides its data as the output data.

15. The cache memory of Claim 13, wherein the way select signals selectively disable corresponding cache blocks by forcing corresponding match signals to a mismatch condition.

16. The cache memory of Claim 12, wherein the memory devices comprise fuses.

17. The cache memory of Claim 12, wherein the gating circuits comprise AND gates.